Patent
Attorney's Docket No. H1420

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	
	)	
Shibly S. Ahmed et al.	)	Group Art Unit: Unassigned
	)	
Application No.: Unassigned	)	Examiner: Unassigned
	)	
Filed: January 12, 2004	)	
	)	
Title: DAMASCENE TRI-GATE FINFET	)	

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

U.S. Patent and Trademark Office
2011 South Clark Place
Customer Window
Crystal Plaza Two, Lobby, Room 1B03
Arlington, Virginia 22202

Sir:

Pursuant to 37 C.F.R. §§ 1.56 and 1.97(b), Applicant(s) bring to the attention of the Examiner the documents listed on the attached PTO 1449. This Information Disclosure Statement is being filed before the mailing date of a first Office Action in the above-referenced application. As such, no certification or fee is required. Copies of the listed documents, except for U.S. Patents and U.S. Patent Publications, are attached.

Applicant(s) respectfully request(s) that the Examiner consider the listed documents and indicate that they were considered by making appropriate notations on the attached form.

If any copending application(s) is/are cited on the attached PTO 1449, the Examiner's attention is directed to the foregoing application(s) in compliance with § 2001.06(b) of the Manual of Patent Examining Procedure. By identifying the copending application(s), the assignee and/or applicant of the application(s) do not waive confidentiality of the application(s). Accordingly, the U.S. Patent and Trademark Office is requested to maintain the confidentiality of the copending application(s) under 35 U.S.C. § 122.

This submission does not represent that a search has been made and does not constitute an admission that each or all of the listed documents are material or constitute "prior art." If the Examiner applies any of the documents as prior art against any claim in the application and Applicant(s) determine(s) that the cited document(s) do not constitute "prior art" under United States law, Applicant(s) reserve(s) the right to present to the Office the relevant facts and law regarding the appropriate status of such documents.

Applicant(s) further reserve(s) the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 50-1070.

Respectfully submitted,

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Date: January 12, 2004

INFORMATION DISCLOSURE CITATION PTO-1449	Customer Number: 26615	ATTORNEY'S DKT NO. H1420	APPLICATION NO. Unassigned
		APPLICANT(S) Shibly S. Ahmed et al.	
		FILING DATE January 12, 2004	GROUP Unassigned

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	6,583,469	06-24-03	Fried et al.	257	329	01-28-02
	6,562,665	05-13-03	Yu	438	149	10-16-00
	6,551,886	04-22-03	Yu	438	300	04-27-01

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation Yes	Translation No
	WO 03/015182	02-03	WIPO				

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	Digh Hisamoto et al., "FinFET-A Self-Aligned Double-Gate MOSFET Scalable to 20 nm," IEEE Transactions on Electron Devices, Vol. 47, No. 12, December 2000, pages 2320-2325.
	Yang-Kyu Choi et al., "Sub-20nm CMOS FinFET Technologies," 2001 IEEE, IEDM, pages 421-424.
	Xuejue Huang et al., "Sub-50 nm P-Channel FinFET," IEEE Transactions on Electron Devices, Vol. 48, No. 5, May 2001, pages 880-886.
	Xuejue Huang et al., "Sub 50-nm FinFET: PMOS," 1999 IEEE, IEDM, pages 67-70.
	Yang-Kyu Choi et al., "Nanoscale CMOS Spacer FinFET for the Terabit Era," IEEE Electron Device Letters, Vol. 23, No. 1, January 2002, pages 25-27.
	Co-pending U.S. Application No. 10/320,536 filed December 17, 2002 entitled: "FinFET Gate Formation Using Reverse Trim of Dummy Gate," 14 page specification, 11 sheets of drawings.
	Co-pending U.S. Application No.10/459,589 filed June 12, 2003 entitled: "FinFET Gate Formation Using Reverse Trim and Oxide Polish," 17 page specification, 28 sheets of drawings.
	Co-pending U.S. Application No. 10/310,777 filed December 6, 2002 entitled: "Damascene Gate Process with Sacrificial Oxide in Semiconductor Devices," 19 page specification, 10sheets of drawings.
	Co-pending U.S. Application No. 10/645,577 filed August 22, 2003 entitled: "Sacrificial Oxide Protection During Dummy Gate Removal in Damascene Gate Process in Semiconductor Devices," 19 page specification, 9sheets of drawings.

EXAMINER	DATE CONSIDERED

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	6,551,885	04-22-03	Yu	438	300	02-09-01
	6,525,403	02-25-03	Inaba et al.	257	618	09-24-01
	6,515,320	02-04-03	Azuma et al.	257	288	11-08-01
	6,475,890	11-05-02	Yu	438	574	02-12-01
	6,458,662	10-01-02	Yu	438	286	04-04-01
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	6,406,951	06-18-02	Yu	438	183	02-12-01
	6,342,410	01-29-02	Yu	438	164	07-10-00
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	US2003/0111686	06-19-03	Nowak	257	328	12-13-01

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EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation Yes	Translation No

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